Abstracts

Design and analysis of a multi-layer transformer balun for silicon RF integrated circuits (2002 [RFIC])

H.Y.D. Yang, L. Zhang and J.A. Castaneda. "Design and analysis of a multi-layer transformer balun for silicon RF integrated circuits (2002 [RFIC])." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 491-494.

In this paper, we present the design and analysis of an on-chip transformer balun for silicon RFICs. Both the primary and secondary spread over four metal layers along a common symmetric axis to reduce the overall area, maintaining reasonable quality factor. A five port transformer balun circuit model is developed to facilitate the device simulation. A 4:11 transformer balun is fabricated and tested. It is ideal for LNAs to enhance the gain with optimum noise figure.

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